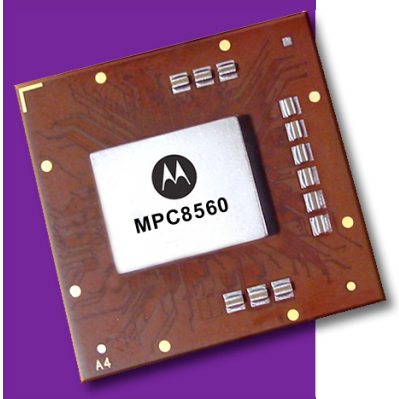
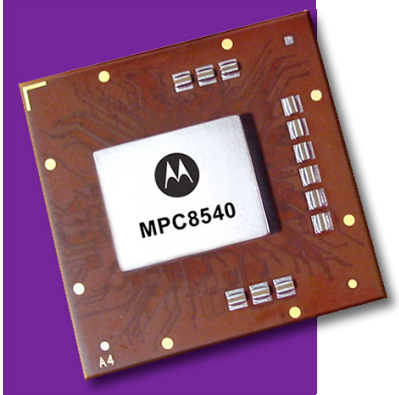
MPC8560/40
PowerQUICC III®
Integrated Communication
Processor

PhoenixMicro Presents:
MPC8560/40 Architectural Training Class

PhoenixMicro Inc.
http://www.phxmicro.com

"Designing with the MPC8560/40"





PhoenixMicro Incorporated, in association with **Freescale Semiconductor** (formerly known as Motorola SPS), is pleased to provide our 5-day MPC8560 training course: **Designing with the MPC8560/40**. We are confident you will learn solid application knowledge designing and developing embedded systems based on the MPC8560/40 Integrated Power PC processors series.

Designing with the MPC8560/40 is exceptionally challenging and a thorough understanding of its architecture and functionality is needed to have a successful design. **PhoenixMicro, Inc.** with our combined experience of over 30 years in the embedded industry offers training and consulting focusing on PowerPC® microprocessors, and other embedded PowerPC micro controllers. We have continually worked with Freescale technical training group for over seventeen years to ensure complete, accurate, and current information. With over thousands of students trained, PhoenixMicro is well qualified to assist designers in their quest to acquire technical knowledge of MPC8560/40 system on a chip.

Audience

The MPC8560/40 PowerQUICC III training course is designed for software, hardware, firmware, test engineers, and developers who want to build communication and networking applications. System architects, project leaders, and BSP designers, device driver designers, test engineers who want to understand device architecture and requirements are also encourage to attend the class for an in-depth understanding of the silicon system.

Prerequisite

Understanding of MPC8260, or MPC8xx is helpful. Also, familiarity with C language especially data structure organization is advantageous. However, student's willingness and desire to learn is the most important factor.

PhoenixMicro Inc.
Bringing simplicity to a complex environment

Contents:

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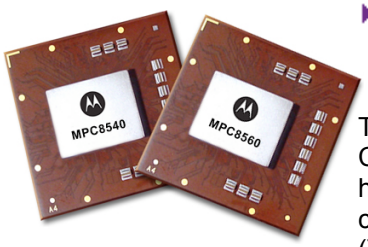

MPC8560/40 PowerQUICC III Integrated Communication Processor System

The MPC8560/40 PowerQUICC III (Power Quad Integrated Communications Controller - Third Generation) is a single-chip, highly integrated microcontroller. It has a 32-bit RISC PowerPC e500 core (5th generation) as a host processor, a communication processor module (CPM), two triple speed Ethernet controllers (TSEC), DDR SDRAM memory controller, 64-bit PCI-X/PCI controller, RapidIO™ interconnect and much more.

"Designing with the MPC8560/40" course agenda:

The class that will cover both the hardware and software aspect of the device. Each topic is self-contained. That is, both hardware and software materials are included to make the topic complete. The class consists of lectures and exercises.

- Overview of the overall functional description of the MPC8560 and MPC8540 architectures.
- Understand the MPC8560/40 internal memory map structure and inbound/outbound window mapping and address translation operation.
- Learn the latest e500 core programming model, register types, and usages.
- Review e500 core instruction set, branches, subroutine calls, simplified mnemonics, and accessing operand in memory.
- Write efficient exception service routines to the new e500 programmable interrupt controller (PIC) by understanding the innovative exception processing function with built-in interrupt priorities and separate critical interrupt path.
- Configure and optimize the e500 L1 caches and the L2 look-aside cache/static SRAM block to suit your application.
- Initialize the new Motorola Book E two-level MMU architecture to perform address translation and enable access control and protection.
- Configure the dual TSEC for 10/100/1000 Mbps Ethernet operation.
- Understand the RapidIO™ open standard and the RapidIO™ interconnect controller operation.
- Configure and initialize the advanced DDR SDRAM memory controller.
- Program and initialize the DMA controller to transfer data between RapidIO and local address spaces.
- Configure and initialize the 64-bit PCI-X/PCI controller module.
- Program the CPM FCC module to transmit and receive HDLC packets, transmit and receive Ethernet frames, and transmit and receive ATM cells.
- Program and initialize a second memory controller via Local Bus Controller (LBC) for local bus functions for SDRAM (DRAM), SRAM, flash EPROM, and EPROM memory operations.
- Configure and initialize the CPM Time Slot Assigner (TSA) for time division multiplexing (TDM).
- Program the CPM Multi-Channel Controller (MCC) for HDLC or Transparent protocol for up to 128 channels per MCC.
- Learn how to initialize the MPC8560/40 from power-on reset.

Note: Total topics covered will vary depending on class size, student's background, and pace of the class. Our instructors are flexible to adapt and adjust topics to suit the requirements. **We do both open class and on-site class training**.

Launched by Motorola freescale semiconductor

"Training today for tomorrow's success."

For open classes near your area visit us at:

http://www.phxmicro.com/Schedule/index.htm